therefor the following:

A first transistor formed in a peripheral circuit portion of a semiconductor substrate. The first transistor includes source and drain diffusion layers formed in one element region. A5 A second transistor formed in a memory cell portion of the semiconductor substrate. The second transistor includes source and drain diffusion layers in another element region. A contact connected to the one of the source and drain diffusion layers. A first insulating film different from a silicon oxide covers the second transistor. The first insulating film is an etching stopper for the contact to the element isolation region and has a property which makes it difficult for an oxidizing agent to pass therethrough compared with the silicon oxide.

REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-3, 5, 11-14, and 19-25 are presently active. Claim 4 has been canceled without prejudice; Claims 1-3 and 11-14 have been amended; and Claims 19-25 have been added by the present amendment. Claims 6-10 and 15-18 stand withdrawn. The changes to the claims are supported by the originally filed specification and do not introduce any new matter.

In the outstanding Office Action, Claims 1-3 and 5 were rejected under 35 U.S.C. §102(b) as being anticipated by or, in the alternative, under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,495,693 to Iwahashi et al. (hereinafter "the '693 patent"); Claims 4, 11, and 14 were rejected under 35 U.S.C. §103(a) as being unpatentable over the '693 patent in view of U.S. Patent No. 4,866,003 to Yokoi et al. (hereinafter "the